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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,867	03/17/2004	Jun Otsuka	Q79598	1991

23373 7590 08/30/2006

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EXAMINER	
HA, NGUYEN T	

ART UNIT	PAPER NUMBER
2831	

DATE MAILED: 08/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,867	OTSUKA ET AL.	
	Examiner	Art Unit	
	Nguyen T. Ha	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *6-7 and 11-22* is/are withdrawn from consideration.

5)☒ Claim(s) *5 and 8-10* is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0304 & 0404*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-5 and 8-10 in the reply filed on 6/26/2006 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Chakravorty et al. (US 6,775,150).

Regarding claim 1, Chakravorty et al. disclose a capacitor (figures 1-3) comprising:

- an approximately plate-shaped capacitor main body (90) having a first surface on which a semiconductor device (60) having surface-connecting terminals (121 & 125) is to be mounted and a second surface; and
- a plurality of electrically conductive vias (143 & 153) penetrating the capacitor main body (90) between the first and second surfaces for connection with the surface connecting terminals.

Regarding claim 2, Chakravorty et al. disclose a semiconductor device equipped capacitor assembly (figures 1-3) comprising:

- a semiconductor device (60) having surface-connecting terminals (121 & 125); and
- a capacitor (90) having an approximately plate-shaped capacitor main body having a first surface on which the semiconductor device is mounted and a second surface and a plurality of electrically conductive vias (143 & 153) penetrating the capacitor main body between the first and second surfaces and connected to the surface-connecting terminals.

Regarding claim 3, Chakravorty et al. disclose a capacitor equipped substrate assembly (figures 1-3) comprising:

- a substrate (200) having surface-connecting pads (201, 203, 205); and
- a capacitor main body (90) having a first surface and a second surface at which the capacitor is mounted on the substrate and a plurality of electrically conductive vias (143, 153) penetrating the capacitor main body between the first and second surfaces and connected to the surface-connecting pads (figure 3).

Regarding claim 4, Chakravorty et al. disclose an assembly comprising:

- a semiconductor device (60) having surface-connecting terminals (121, 125);
- a substrate (200) having surface-connecting pads (201, 203, 205); and

- a capacitor (90) having an approximately plate-shaped capacitor main body having a first surface on which the semiconductor device is mounted and a second surface at which the capacitor main body is mounted on the substrate and a plurality of electrically conductive vias (143, 153) penetrating the capacitor main body between the first and second surfaces and connected to the surface-connecting terminals and the surface-connecting pads (figure 3).

Allowable Subject Matter

4. Claims 5 and 8-10 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claim 5, the prior art alone or in combination does not teach the limitation of an interposer comprising an interposer main body having a first surface on which a semiconductor device (60) having surface-connecting terminals is mounted and a second surface formed with a recess, and a plurality of interposer main body side electrically conductive vias penetrating the interposer main body between the first surface and a bottom surface of the recess and connected to the surface-connecting terminals; and

With respect to claim 8, the prior art alone or in combination does not teach the limitation of a semiconductor device equipped interposer assembly comprising: an interposer main body having a first surface on which the semiconductor device having surface-connecting terminals is mounted and a second surface formed with a recess, and capacitor disposed in the recess and having front and rear surfaces and a plurality

of capacitor side electrically conductive vias extending through the front and rear surfaces.

With respect to claim 9, the prior art alone or in combination does not teach the limitation of an interposer equipped substrate assembly comprising an interposer having a plurality of interposer main body side electrically conductive vias penetrating the interposer main body between first and second surfaces and connected to the surface-connecting terminal and a capacitor disposed in the recess.

With respect to claim 10, the prior art alone or in combination does not teach the limitation of an assembly comprising an interposer having an approximately plate shaped interposer main body having a first surface on which the semiconductor device is mounted and a second surface formed with a recess, and the interposer further having a plurality of interposer main body side electrically conductive vias penetrating the interposer main body between the first surface and a bottom surface of the recess and connected to the surface-connecting terminals and a capacitor disposed in the recess.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Citation Relevant of Prior Art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Figueroa et al. (US 6,532,143) disclose multiple tier array capacitors.

b. Kubota et al. (US 6,183,669) disclose paste composition, circuit board using the same, ceramic green sheet, ceramic substrate, and method for manufacturing ceramic multilayer capacitor.

c. Malladi (US 5,939,782) discloses package construction for integrated circuit chip with bypass capacitor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen T. Ha whose telephone number is 571-272-1974. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NGUYEN T. HA
PRIMARY EXAMINER

NH
August 25, 2006